An Investigation into the Design Parameters of Booth's Multiplier: A Comparative Approach

Tariq Ali[*1], Ahmed Khan[*2] and Fatima Zahra[*3]

[*1]Department of Mechanical Engineering, University of Karachi, Karachi, Pakistan
[*2]Department of Civil Engineering, NUST University, Islamabad, Pakistan
[*3]Department of Electrical Engineering, COMSATS University, Islamabad, Pakistan

ABSTRACT

In digital signal processing applications, one of the critical parameter in digital system design is performance. The IC's used in digital signal processing applications consume majority of IC power. Nearly 15 to 20 % of IC power is consumed by multiplication alone. A part from design, speed of operation and area are key requirement. In this paper different type of multipliers are compared in terms of design parameters. Booths multiplier offers several advantages over other type of multipliers in terms of area, power consumption and speed can further be improved using modified booths algorithm.

KEYWORDS: Array multiplier, Wallace tree multiplier, Vedic multiplier, booths multiplier

I. INTRODUCTION

Multipliers play an integral part in modern electronics and other different types of applications. The need for low power VLSI system arises from two main reasons. Firstly, with the study growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat generated must be removed by proper cooling techniques. Secondly, battery life in portable electronic devices is limited and low power design directly leads to prolonged operation time. Extensive work is being carried out on low power multipliers at technological, physical, circuit and logic levels and as a result, several parallel multipliers are designed with different area-speed constraints. During the design of any device we need to keep in mind various parameters like speed of device, area of device, time consuming by device to performance this process, also regularity of the layout and power consumed by this device to perform this process. These all parameters are necessary to obtain the best processing design. For this we use various types of multipliers to perform process in VLSI implementation. As in a device we have to do lot of arithmetic processes like addition, subtraction and multiplications but among all multiplication is very important because the important path is found more by multipliers as it needs highest delay in all basic functional blocks in digital system [1]. Also it need lot of time as compared to other operation and also needs more hardware device. So to obtain better results in process we need to focus on multipliers because they help a lot in improvement of device performance. Various types of factors are there that help in making electronic design taking consideration of low power dissipation and faster speed. Nowadays many researchers have started working on multipliers design with high efficiency and the only purpose of it is to provided high speed and low power dissipation. This helps these multipliers well suited for different movable and difficult VLSI circuit implementations. In multipliers twin precision method is used to get dual output [2]. Multiplier architecture is divided into 3 parts: creation of partial product, summing of partial product and final addition. Block Diagram of multiplier architecture is shown in figure below. [3]

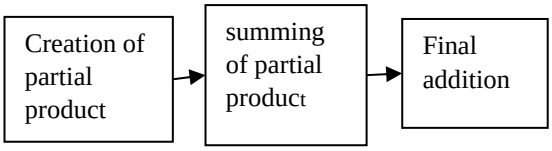

Figure 1: Architecture of multiplier

Digital multiplication does the process of addition of partial products in a particular order. Process by which addition of partial product array is done to provide the final result is the important distinctive reason between several multiplications. Figure below show how process is done on partial product array.

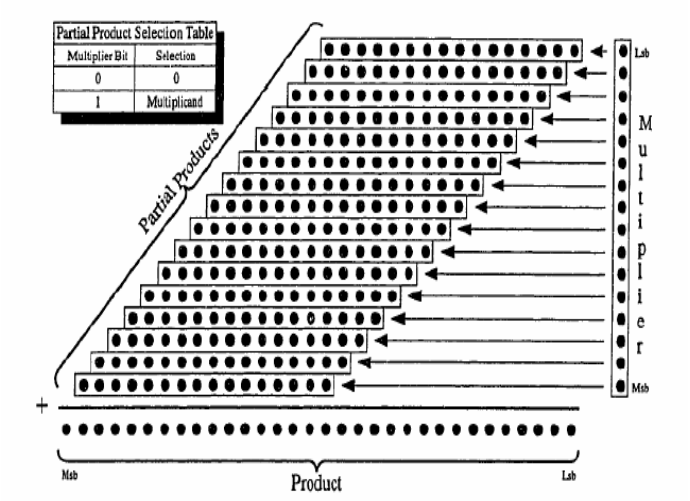

Figure 2: 16 bit partial product array

Different types of multipliers are there and these are classified as given below. Multipliers are classified on the basis of serial and parallel multipliers.

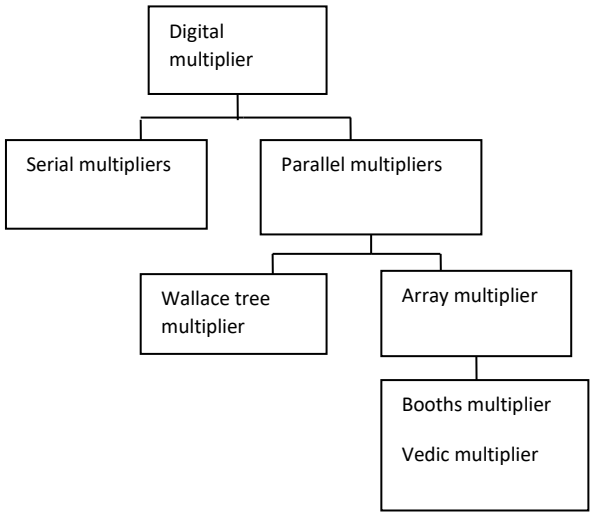

Figure 3: Digital multiplier classification

Multiplication can be done using two multipliers like serial multipliers and parallel multipliers as shown below.

- **Serial multiplier**

Serial multiplier is the easy and simple type of multiplier but the process done is quit slow as the output we get in it is only after m clock cycles, where m is size of operands. Serial multipliers are considered only when the area and power is not necessary in device and also excess in delay is avoided.

- **Parallel multiplier**

Faster version of this serial multiplier can be achieved by adding partial products at single time. We can get this by unfolding the serial multiplier and achieve a combinational circuit in which there are several partial product generators mixed with several adders which perform in parallel. The multiplier which we get from that is called Parallel Multiplier and is shown in fig below

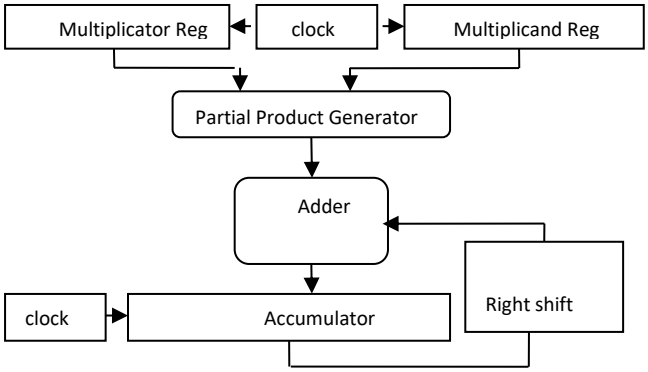

Figure 4. Serial type multiplier

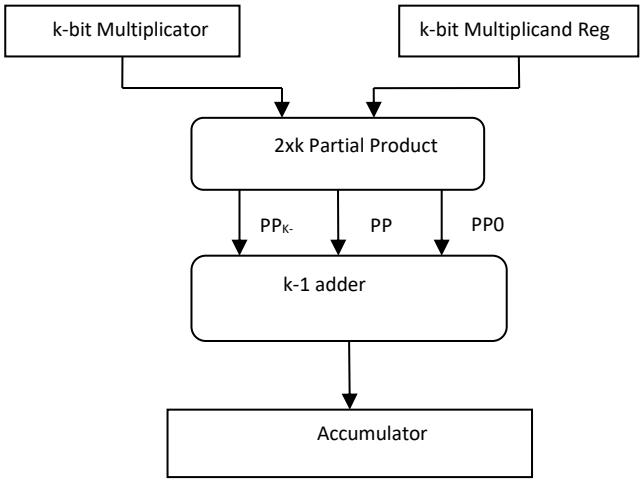

Figure 5. Parallel type multiplier

II. ARRAY MULTIPLIERS

Array multipliers are important because it has simple and regular layout of combinational circuit so process in it is simple. In this we use and gate to obtain partial product and we use m x (m-2) full adders and m half adders. In this type of multiplier each of the product bit is fed to the full adder which add this product bit to the adder which we get previously and also to the carry of the least significant of the adder which we get before that. This process is done in rows and the length of multiplier is obtained by counting how many rows are used in this array multiplier also the thickness of multiplicand is achieved by thickness of each of the row of array multiplier. This type of multiplier is designed using following steps. Here the array multiplier of 16*16 bit is simulated using Xilinx 8.1 tool [4]. The procedure of to design this multiplier is given below as step by step;

Here multiplier circuit is simply processed through add and shift algorithm. Partial product is obtained by the process of multiplication of the multiplicand with single multiplier bit. Then there is a process of shifting and their procedure is done according to bit order and after that it is added. Addition in this is done through very simple method using simple carry propagate adder. M-1 adders are needed where M denote length of the multiplier.

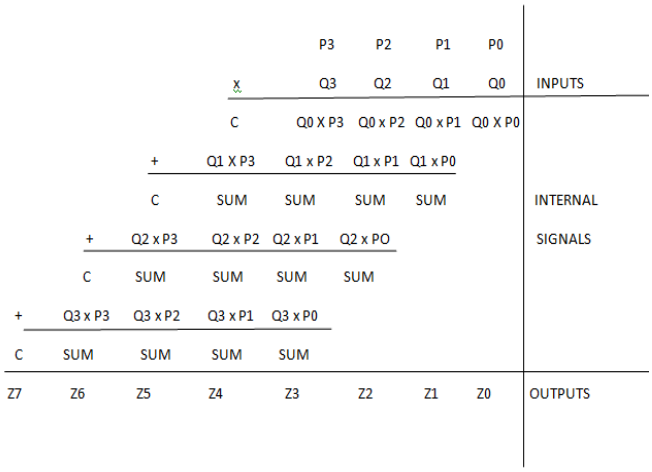

Figure 6: Structure of array multiplier

Algorithms used in are variables for multiplicand and multipliers, shift and add processes. But there are few demerits in array multiplier also as area is small in it also circuit complexity is also simple in it but it has some problems that it is low speed algorithm also power consumption is high in array multiplier[5]

III. VEDIC MULTIPLIERS

Vedic multipliers play a vital role in multiplication process as there are large no of arithmetic operation in process and these operations are time consuming which decreases the speed of the multiplier. So to avoid this Vedic multipliers play an important role. It had become important method for quicker calculation and examination [11]. It is considered as the quickest and lower in terms of power as compared to array and booth multipliers [12]. This term has been obtained from Vedic mathematics which is anciently used in mathematics in India. As Vedic is treated as store house of information. [13]Vedic multiplier is composed of total 16 algorithms for various types of logic operations but among these algorithms vertically crossover method is considered most as it has lot of properties as compared to other 15 algorithms in terms of complexity as this algorithm is simple, better and is not complicated as compared to other algorithms[14]. Also speed of this algorithm is resourceful as compared to other 15 algorithms. Vertically crossover process is done by this way as shown below [15]. Let's take 2 numbers 30 and 27 how process is done in it is shown below:

30 X 27 = 810

3 0

2 7

Now we considered LSB of these two numbers and then multiply them with each other. After completion of process the result we get will become the LSB of the answer.

Now in 2nd step we take these both numbers and then multiply them horizontally and then add these both together after that LSB of this output carried to the left of the first and the MSB bit is carried to the next step.

3 0

2 7

21 +0= 21

Now in final step we take MSB of these two numbers and then multiply these both numbers. Output of these two numbers are added by previous MSB of the process.

3

2

6 + 2 = 8

So from above example it is clear that Vedic multiplier is better as compared to array multiplier as the partial product is done in it parallel. So speed of this multiplier is considered as higher as compare to array multiplier.

IV. BOOTH'S MULTIPLIERS

Booths multiplier was IST given by Andrew Donald booths in year 1950[16]. Booths algorithm can work low when count of partial products is high because it to perform all sums IST after that output can be generated. Function of this booths multiplier is to provide method for multiplying binary integers in signed 2's complement illustration. Hardware multiplication is same as other multiplication process like partial products are determined, shifting and summing process. Booths multiplication method is basically done by two shifting processes one is arithmetic and other one is circular. Circular shift is done by this process IST then numbers are kept in an arranged manner. After that shifting is done by two ways left circular or right circular shift operation. In left circular operation IST digit is reversely shifted to last digit and the rest bits are shifted 1 bit left. While in right shift circular operation last bit is shifted forward to IST bit and remaining bits are shifted to right one bit. In this way circular shifting is done in it. The algorithm of Booth's Multiplier is given as under:

In this registers S and R are used to kept multiplicand and multipliers respectively. 1 bit register B is kept right of LSB R0 of R register. It is represented by R-1. At IST B and R-1 are set to 0. Now In this further process is done by check two bits and decision is made according to that. If both bits are same like 11 or 00 then at that time all bits of B, R, R-1 are shifted to right once. Now if combination of bits is 10 at that time subtraction process is done in which multiplicand is subtracted from B. And if combination gives 01 that time addition process is done multiplicand is added to B. In both cases the output is stored in B, also after both these addition and subtraction operation B, R, R-1 are shifted towards right. This is called arithmetic shift operation. In this sign of numbers B and R are protected. Output of multiplication comes out in B and R.

But booths multiplier takes more area for operation, power consumption is low and speed is almost same as array multiplier. Maximum number of adder cells are used by booths multiplier to provide high quality output but it has a problem that it consumes more power [17],[18]. So we prefer modified booths algorithm as compared to this so that area is reduced delay is also minimized [19].

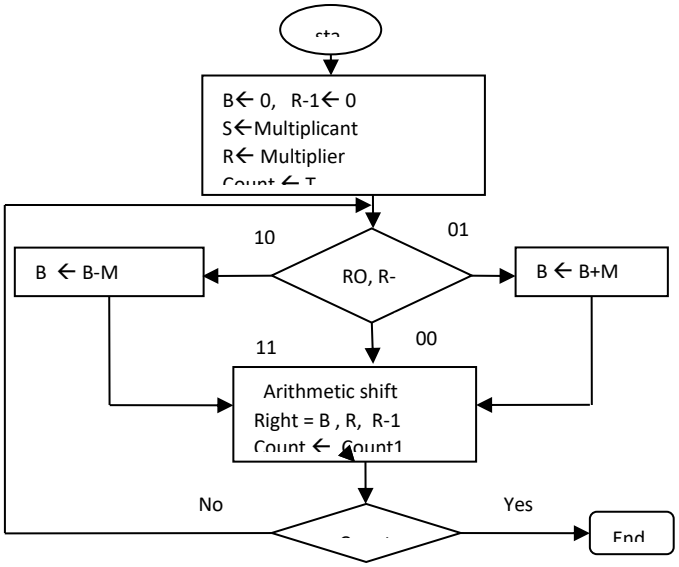

Figure 8:- Design flow of Booth algorithm

V. RESULTS AND DISCUSSION

Table 2: Specification of Wallace tree type.

	Wallace Tree
17-bit adder	9
17-bit subtractor	9
5-bit subtractor	1
1-bit register 33-bit register 5-bit register	4 1 2
1-bit 8-to-1 MIX 33-bit 2-to-1 MUX	17 2
Flip-Flops	34
Delay	12.932ns (11.728ns logic, 1.204ns route) (58.9% logic, 41.1% route)

Table 1: Specification of Array type.

	Array16-bit
Adders/Subtractors	15
32-bit adder	15
32-bit 2-to-1 multiplexer	16
Delay:	21.206 ns 206ns (Levels of Logic = 63) 21.206ns (12.743ns logic, 8.463ns route) (60.1% logic, 39.9% route)

Table 3: Specifications of Vedic

	Vedic 16 bit
Adders/Subtractors	4
16-bit adder	4
16-bit / 4-inputs adder tree	1
16-bit 8-to-1 multiplexer	4
Delay	13.701ns (6.612ns logic, 7.089ns ro) (43.4% logic, 56.6% route)

Table 4: Specifications of Booth's Multiplier

	Booth 16bit
32-bit adder	8
3-bit comparator greater	7
32-bit 2-to-1 multiplexer	7
32-bit 8-to-1 multiplexer	8
4-bit 2-to-1 multiplexer	3
Delay	12.701ns (5.612ns logic, 7.089ns route) (48.3% logic, 51.7% route)

VI. CONCLUSION

On comparsion of various multipliers array multiplier has low complication and area is also low but it has difficulty that it has low speed and power utilization is higher as compared to other multipliers. On the other hand wallace tree multiplier has speed superior than array multiplier and also power utilization is also less as compared to array multiplier but area in it is huge. Vedic multiplier has lesser power consumption and complexity less it also has higher speed but it has area larger than booths multiplier. Booths multipliers has both area and power consumption less. Speed is also excellent in booth multiplier. But to make area more smaller as compared to booths and other multiplier we prefer modified booths multiplier to make more less area process.

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